REMARKS

Claim Rejections Under 35 USC §103

Claims 24-36 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586), Akram et al. (US Patent No. 5,739,585) and Hoffman et al. (US Patent No. 5,360,942).

Summary of the Invention

Claims 24-36 are directed to a board-on-chip semiconductor package 62 (Figure 6B). As shown in Figure 6B, the BOC package 62 includes a substrate 56 comprising a first surface 44 with a pattern of conductors 48, an opposing second surface 46 with a die attach area 50, and a wire bonding opening 64 extending through the substrate 56 from the first surface 44 to the second surface 46. In addition, the package 62 includes a first solder mask 80A on the first surface 44, and a second solder mask 80B on the second surface 46 having an opening 86 (Figure 3D) on the die attach area 50.

As also shown in Figure 6B, the package 62 includes a semiconductor die 16 placed face down (circuit side down) in the opening 86 in the second solder mask 80B, and attached directly to the substrate 56 in the die attach area 50. An adhesive layer 72 (Figure 6A) attaches the face of the die 16 directly to the substrate 56. The package 62 also includes wires 94 in the wire bonding opening 64 bonded to bonding pads on the face of the die 16, and to bonding pads 52 (Figure 6A) on the conductors 48. As also shown in Figure 6B, an encapsulating resin 90 is molded over the die 16, and over the second solder mask 80B.

Rejections Under 35 USC §103

The rejections under 35 USC §103 are traversed as the claims "taken as a whole" are submitted to be unobvious over the combination of references "taken as a whole". In addition, one skilled in the art at the time of the invention would have no reason to combine the references in the manner of the Office Action.

The APA discloses a BOC semiconductor package 10 (Figure 1A) that includes a substrate 12 having an opening 26 there through, a die 16 on the opening 26 face bonded to a solder mask 20B on the substrate 12, and wires 28 in the opening bonded to the die 16 and to conductors 18 on the substrate 12.

Lee et al. discloses a substrate board 200 (Figure 3) having a solder mask 218 with a die attach area 204 (Figure 3). As shown in Figure 6 of Lee et al., the die 220 is back bonded to the die attach area 204, and wire bonded to conductors 202 (Figure 4) on the substrate board 200.

Akram et al. discloses a semiconductor package 10FR (Figure 10) having a substrate 12FR and a die 18 face bonded to the substrate 12FR using an adhesive layer 23FR.

Shim et al. discloses a semiconductor package comprising a PCB 7, and a semiconductor chip 1 back bonded to the PCB 7 using a heat conductive epoxy resin 3.

Hoffman et al. discloses a semiconductor package having a substrate 20, and a semiconductor device 26 bonded to the substrate 20 using a thermally conductive die attach 40 (Figure 3).

The test for combining references is not what individual references themselves suggest but rather what the combination of disclosures taken as a whole would have suggested to one of ordinary skill in the art at the time of the invention. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). In addition, the examiner must provide reasons why one of ordinary skill in the art would have been led to

combine the prior art references to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

The Office Action identifies the reason for the combination as: "so that the die is bonded directly to the second surface using a filled adhesive so that the bonding and heat transfer from the chip to the substrate can be improved and the encapsulation defects can be reduced using Lee et al., Akram et al. and Hoffman's bonding structure in the admitted prior art."

However, there is no teaching in the combination of references that the bonding of a die to a substrate is improved by an open die attach area. Although the die 220 in Lee et al. may have improved bonding because of the die attach area 204 not being covered by the solder mask 218', Applicant is unable to locate any disclosure in Lee et al. that specifically teaches this result. As the improved bonding teaching is not in the art, it is not a valid reason for the proposed combination of references. Further, even though this teaching is contained in the present disclosure, it cannot be used against the Applicant to support a 35 USC §103 rejection. As held in Orthopedic Equipment Co. v United States, 702 F2d 1005, 217 USPQ 193 (Fed. Cir. 1983): "It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit."

With respect to the heat transfer reason for the proposed combination, filled adhesives, as exemplified by Shim et al. and Hoffman et al., are admittedly known in the art. However, independent claims 27 and 30 state that the filled adhesive layer "transfers heat directly from the face to the substrate". In Shim et al. and Hoffman et al. the dice are back bonded to the filled adhesive. No art has been cited in which a filled adhesive on the face of a

die is used to transfer heat directly from the face to the substrate. Integrated circuits on a die are located next to the face rather than to the back side of the die, such that most of the heat in the die is generated at the face. In the presently claimed package, the filled adhesive layer in direct contact with the face of the die and with the substrate, provide an improved heat transfer mechanism and improved bonding, which is not taught by the combination of references.

Further, Applicant respectfully disagrees with the statement in the Office Action "that encapsulating defects can be reduced using Lee et al., Akram et al. and Hoffman's bonding structure in the admitted prior art". In this regard, Lee et al. teaches that "if encapsulating materials remain over gate area 252 after the encapsulating material hardens, it may be easily (e.g., de-gated) without damaging the solder mask 218' (column 8, lines 13-16)". In Lee et al., there are fewer encapsulating defects because the gate area 252 (Figure 7) comprises polyimide, rather than gold (column 8, lines 11-12), and not because of the open die attach area 204. Further, the presently claimed package does not use a polyimide gate area for the encapsulant, but rather uses "square metal segments 76" (page 9, lines 24-26). As with the improved bonding and heat transfer reasons for combining the references, the "reduced encapsulating defects" reason is also not supported by the art.

As with the combination of references, in assessing unobviousness the claims must also be "taken as a whole". In this regard, Applicant submits that the recitations in independent claims 24, 27, 30 and 34 of package having a solder mask with an open die attach area and a face bonded die in combination, makes all of the claim unobvious over art. Applicant further submits that the additional recitations in independent claims 27 and 30 of a filled

adhesive layer and direct heat transfer, makes claims 27-33 further distinguishable from the art.

Conclusion

In view of the above arguments and amendments, favorable consideration and allowance of claims 24-36 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

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March 10, 2003
Date of Signature

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Marked Version Of Amended Claims Showing Changes

24. (six times amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors [and ball bonding pads] on the first surface, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline and a face on the bonding opening bonded directly to the second surface;

a first mask on the first surface;
[comprising a plurality of via openings aligned with the ball bonding pads;]

a second mask covering the second surface except in a die attach area defined by an opening through the second mask having a second outline corresponding to [but only slightly larger than] the first outline;

an adhesive layer between the face and [the substrate in] the die attach area bonding the die to the substrate; [second surface;]

a plurality of wires [placed through] in the bonding opening [and] wire bonded to the die and [to] in electrical communication with the conductors; and

an encapsulating resin on the die and on the second mask.

27. (six times amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors on the first surface, [comprising ball bonding pads and] a plurality of wire bonding pads on the first surface in electrical communication with the conductors, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline and [, the die comprising] a face on the bonding opening bonded to the second surface;

a first mask on the first surface;

[comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;]

a second mask [substantially covering] on the second surface comprising a second opening having a second outline corresponding to [but only slightly larger than] the first outline [to define] defining an open die attach area on the second surface;

a filled adhesive layer between the face and the [substrate in the open] die attach area bonding the die to the [second surface] substrate and configured to transfer [and transferring] heat directly from the face to the substrate;

a plurality of wires in the bonding opening wire bonded to the die and to the wire bonding pads; and

an encapsulating resin on the die and on the second mask.

30. (six times amended) A semiconductor package comprising:

a substrate having a first surface, a second surface and a bonding opening there through;

a plurality of conductors on the first surface having a plurality of wire bonding pads;

a first mask on the first surface at least partially covering the conductors;

a second mask [covering] on the second surface except in a die attach area defined by an opening [through] in the second mask;

a semiconductor die on the die attach area having a face aligned with the bonding opening [and] attached to the second surface;

a filled adhesive layer attaching the [die] face to the [substrate in the open] die attach area and configured to transfer heat directly from the face to the substrate; [second surface;]

a plurality of wires [placed through] in the bonding opening [and] bonded to the die and to the [conductors] wire bonding pads; and

an encapsulating resin on the second mask encapsulating the die.

34. (five times amended) A semiconductor package comprising:

a substrate comprising a first surface, an opposing second surface and a wire bonding opening from the first surface to the second surface;

a plurality of conductors on the first surface comprising wire bonding pads; [and ball bonding pads;]

a first mask on the first surface; [comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;]

a semiconductor die aligned with the wire bonding opening and bonded face down to the second surface, the die having a first outline;

a second mask substantially covering the second surface and including an opening there through having a second outline corresponding to but only slightly larger than the first outline [to define] defining a [an open] die attach area on the second surface;

an adhesive layer between the die and the [substrate in the open] die attach area bonding the die [directly] to the [second surface] substrate;

a plurality of wires [placed through] in the wire bonding opening [and] bonded to the die and to the wire bonding pads; and

an encapsulating resin on the second mask encapsulating the die.